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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/062,044	01/31/2002	Steven Teig	SPLX.P0093	1993

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/062,044	TEIG ET AL.	
	Examiner	Art Unit	
	Naum B Levin	2825	

-- Th MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19, 27-36 and 44-46* is/are rejected.

7)☒ Claim(s) *20-26 and 37-46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/062,044 and Amendment filed on 03/26/2003. Claims 1-46 remain pending in the application.

Examiner appreciates the detailed remarks offered by Applicant. Based on the remarks and Amendment Examiner has performed additional search, and found a new references.

Claim Objections

2. Claims 1, 6, 31 and 44 are objected to:

the recitation of "output functions", is not clear to what applicants intend to mean.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-18, 27-36 and 44-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Belkhale et al. (US Patent 6,023,566) in view of Khouja et al. (US Patent 5,696,694).

Belkhale discloses cluster matching for circuit implementation including:

(1), (44) A method for producing a circuit description of a design, the method comprising:

a) from the design selecting a candidate sub-network (col.2, ll.1-5 and ll.55-57);

b) identifying output functions/Boolean functions/signatures performed by the candidate sub-network (col.2, ll.12-27 and ll.33-38; col.4, ll.33-50; col.5, ll.55-67; col.6, ll.1-11 and col.8, ll.6-28);

c) based on the identified output functions/Boolean functions/signatures, retrieving/choosing a replacement sub-network from a storage structure that stores replacement sub-networks/technology library/cells in the library (col.5, ll.2-54);

d) determining/evaluating whether to replace the selected candidate sub-network with the replacement sub-network in the design (col.6, ll.12-51 and col.7, ll.25-42);

e) if determine to replace the selected candidate sub-network, replacing the selected candidate sub-network with the replacement sub-network in the design (col.5, ll.2-6 and col.7, ll.25-54);

(2) The method of claim 1, wherein the output functions includes only one output function (col.4, ll.33-50);

(3) The method of claim 1, wherein the output functions includes a plurality of output functions (col.2, ll.12-27; ll.33-38; col.4, ll.33-50; col.5, ll.55-67 and col.6, ll.1-12);

(4), (45) The method of claim 1, wherein the candidate sub-networks includes multiple circuit elements (col.4, ll.33-50 and col.5, ll.2-54);

(5), (46) The method of claim 1, wherein the storage structure stores sub-networks up to a particular complexity (col.4, ll.13-22 and ll.33-50);

(6), (16), (31), (35) A method and computer readable medium storing a computer program for producing a circuit description of a design, the method comprising (col.3, ll.66-67 and col.4, ll.1-12):

a) from the design, selecting a candidate sub-network that performs output functions, wherein the candidate sub-network includes a circuit elements (col.2, ll.1-5, ll.12-27, ll.33-38 and ll.55-57; col.4, ll.33-50; col.5, , ll.2-54 and ll.55-67; col.6, ll.1-11 and col.8, ll.6-28);

b) generating a parameter/Boolean function based on the output functions (col.5, ll.2-54);

c) using the parameter to retrieve a replacement sub-network from a storage structure that stores replacement sub-networks (col.5, ll.2-54);

d) replacing the selected candidate sub-network with the replacement sub-network in the design (col.5, ll.2-6 and col.7, ll.25-54);

(7), (32) The method and computer readable medium storing a computer program further comprising identifying the output functions performed by the sub-network (col.2, ll.12-27 and ll.33-38; col.4, ll.33-50; col.5, ll.55-67; col.6, ll.1-11 and col.8, ll.6-28);

(8) The method of claim 6, wherein the set of circuit elements includes only one circuit element (Fig. 3A);

(9) The method of claim 6, wherein the set of circuit elements includes at least two circuit elements (col.4, ll.33-50; col.5, ll.2-54 and Fig. 3A);

(10) The method of claim 6, wherein each circuit element of the sub-network has an output, and each circuit element's output provides a result of one output function performed by the selected candidate sub-network (Figs. 3A and 3C);

(11) The method of claim 6, wherein each circuit element of the sub-network has an output, and each output function performed by the selected candidate sub-network is provided at only a circuit-element output that fans out of the sub-network (Figs. 3A and 3C);

(12), (33) The method and computer readable medium storing a computer program comprising:

receiving a local function for each circuit element of the selected candidate sub-network (col.2, ll.12-27 and ll.33-38; col.4, ll.33-50; col.5, ll.55-67; col.6, ll.1-11 and col.8, ll.6-28);

identifying each output function from the received local functions (col.2, ll.12-27 and ll.33-38; col.4, ll.33-50; col.5, ll.55-67; col.6, ll.1-11 and col.8, ll.6-28);

(13), (34) The method and computer readable medium storing a computer program wherein each local or output function is represented in terms of a binary decision diagram ("BDD"), and the sub-network has at least first and second circuit elements, wherein the first circuit element performs a first local function, and the second circuit element performs a second local function, wherein the BDD of a first output function is derived from the BDD of the first local function, and the BDD of a second output function is derived from the BDD's of at least the first and second local functions (col.5, ll.37-67 and col.6, ll.1-51);

(14) The method of claim 6 further comprising:

receiving the design, wherein the design is a combinational-logic network (col.2, ll.1-5 and ll.55-57);

selecting additional candidate sub-networks (col.9, ll.10-33);

replacing some of the selected additional sub-networks with replacement sub-networks retrieved from the storage structure (col.5, ll.2-6 and col.7, ll.25-54);

wherein the replacement of the candidate sub-networks optimizes the combinational-logic network design (col.5, ll.2-6 and col.7, ll.25-54);

(15) The method of claim 6 further comprising

receiving a logical representation of the design (col.1, ll.47-51);

converting the logical representation of the design to a circuit-level representation (col.1, ll.51-55);

wherein selecting the candidate sub-network includes selecting the candidate sub network from the circuit-level representation (col.2, ll.1-5 and ll.55-57);

(17), (36) The method and computer readable medium storing a computer program, wherein using the parameter comprises:

a) identifying each replacement sub-network stored in the storage structure that is associated with each index in the set of indices (col.2, ll.12-27 and ll.33-38; col.4, ll.33-50; col.5, ll.2-67; col.6, ll.1-11 and col.8, ll.6-28); and

b) retrieving each identified replacement sub-network (col.5, ll.2-54);

(18) The method of claim 16, wherein the indices are numerical indices (col.8, ll.58-67 and col.9, ll.1-17);

(27) The method of claim 6 further comprising:

before replacing the candidate sub-network with the replacement sub-network, evaluating whether to replace the selected candidate sub-network with the replacement sub-network (col.6, ll.12-51 and col.7, ll.25-42);

wherein said replacing is based on the evaluation (col.5, ll.2-6 and col.7, ll.25-54);

(28) The method of claim 27, wherein the evaluating comprises computing a cost function (col.6, ll.12-51 and col.7, ll.25-42);

(29) The method of claim 27 further comprising:

selecting additional candidate sub-networks (col.9, ll.10-33);

identifying a replacement sub-network for each selected candidate sub-network (col.2, ll.12-27 and ll.33-38; col.4, ll.33-50; col.5, ll.55-67; col.6, ll.1-11 and col.8, ll.6-28);

evaluating each identified replacement (col.6, ll.12-51 and col.7, ll.25-42);

based on the evaluations, replacing some of the candidate sub-networks with the replacement sub-networks identified for the candidate sub-networks (col.5, ll.2-6 and col.7, ll.25-54);

(30) The method of claim 27,

wherein retrieving the replacement sub-network comprises retrieving several replacement sub-networks, the method further comprising:

evaluating each retrieved sub-network to identify viable/suitable replacement candidates (col.5, ll.12-35);

wherein the replacement sub-network that replaces the candidate sub-network is one of the viable replacement candidates (col.5, ll.2-6 and col.7, ll.25-54).

4. With respect to claim 1-18, 27-36 and 44-46 Belkhale teaches the features above but lacks a method for producing the circuit description using a set/multiple of output functions.

Khouja recites method and apparatus for estimating internal power consumption of a digital circuit represented as netlist including:

identifying a multiple of output functions performed by the candidate sub-network (col.28, ll.35-62; col.35, ll.28-49 and ll.66-67; col.36, ll.1-19; col.107, ll.33-57).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Khouja's teaching regarding the method for producing the circuit description using a set/multiple of output functions and use it in Belkhale's invention to improve timing, area space and power consumption in IC, thereby improving an efficiency of the integrated circuit design.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Belkhale in view of Khouja.

5. With respect to claim 19 Belkhale in view of Khouja teach the features above but lacks a method for producing the circuit description using an indices into relational database, witch is well known in the art at the time the invention was made.

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Belkhale's and Khouja's teaching regarding the method for producing the circuit description using the indices into relational database (for example Oracle database) to improve efficiency of the integrated circuit design.

Allowable Subject Matter

6. Claims 20-26 and 37-43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Khouja et al. (US Patent 5,668,694) describes a method of estimating the toggle rates in a circuit containing sequential elements (flip-flops). This is accomplished by constructing a state element graph for the circuit, breaking cycles in the graph, computing the toggle rate in the combinational logic using the levels in the state element graph, and transferring the toggle rates and probabilities across sequential elements. Transferring the toggle rates and probabilities across sequential elements is achieved by modeling any conventional sequential element as a generic sequential element with additional combinational logic.

Shankar Krishnamoorthy et al. (Article "Boolean Matching of Sequential elements, DAC 1994, p. 691-697) discloses a new technique of recognizing the presence of complex sequential elements including different kinds of flip-flops and complex latches having multiple output functions.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PRIMARY EXAMINER